

**Question No: 1 ( Marks: 1 ) - Please choose one**

The \_\_\_\_\_ RTN describes the overall effect of instructions on the programmer visible registers.

- ▶ **Abstract** [click here for detail](#)
- ▶ Concrete
- ▶ Absolute
- ▶ Basic

**Question No: 2 ( Marks: 1 ) - Please choose one**

The instruction set is of \_\_\_\_\_ importance in governing the structure and function of the pipeline.

- ▶ Least
- ▶ **Primary** [click here for detail](#)
- ▶ Secondary
- ▶ No

**زندگی میں کامیابی کا پہلا راز ہے کہ پریشانیوں سے پریشان مت بنو**

**Question No: 3 ( Marks: 1 ) - Please choose one**

\_\_\_\_\_ is the most general and least useful performance metrics for RISC machines.

- ▶ **MIPS** [click here for detail](#)
- ▶ Instruction Count
- ▶ Number of registers
- ▶ Clock Speed

**Question No: 4 ( Marks: 1 ) - Please choose one**

A \_\_\_\_\_ provides four functions: Select, DataIn, DataOut and Read/Write.

- ▶ ALU
- ▶ Bus
- ▶ Register
- ▶ **Memory Cell** (Page 351)

**Question No: 5 ( Marks: 1 ) - Please choose one**

We can classify or partition the SRC instructions by their overall \_\_\_\_\_ behavior.

- ▶ **Register transfer** [click here for detail](#)
- ▶ Memory transfer
- ▶ Execution
- ▶ Logical

**Question No: 6 ( Marks: 1 ) - Please choose one**

The \_\_\_\_\_ RTN describes detailed register transfer steps in the data path that produce the overall effect.

- ▶ Abstract
- ▶ **Concrete** [click here for detail](#)
- ▶ Absolute
- ▶ Basic

**Question No: 7 ( Marks: 1 ) - Please choose one**

All members of the MC68000 family are \_\_\_\_\_ processors.

- ▶ **32-bit** [click here for detail](#)
- ▶ 16-bit
- ▶ 64-bit
- ▶ 8-bit

**جھوٹ انسان اور ایمان دونوں کا دشمن ہے**

**Question No: 8 ( Marks: 1 ) - Please choose one**

\_\_\_\_\_ Operations refers to a processor that can issue more than one instruction simultaneously.

- ▶ Macro
- ▶ Micro
- ▶ Scalar
- ▶ **Superscalar**      [click here for detail](#)

**Question No: 9 ( Marks: 1 ) - Please choose one**

Exceptions which are \_\_\_\_\_ occur in response to events that are paced by the internal processor clock.

- ▶ Asynchronous
- ▶ **Synchronous**      [click here for detail](#)
- ▶ Internal
- ▶ External

**Question No: 10 ( Marks: 1 ) - Please choose one**

In the hazard detection by hardware, resolved by pipeline stalls, if the instructions are in the adjoining stages, then the hazard must be detected in stage \_\_\_\_\_.

- ▶ 4
- ▶ 2
- ▶ **3**      [click here for detail](#)
- ▶ 1

**Question No: 1 ( Marks: 3 ) - Please choose one**

16k x4 static RAM Chip is arranged in the form of four \_\_\_\_\_ cells.

- ▶ 16x512
- ▶ 32x512
- ▶ 256x512
- ▶ 64x256

(Page 352)

عقل مند کہتا ہے میں کچھ نہیں جانتا جبکہ بے وقوف کہتا ہے کہ میں سب کچھ جانتا ہوں

**Question No: 2 ( Marks: 3 ) - Please choose one**

In a DRAM cell, the storage capacitor will discharge in around \_\_\_\_\_

▶ **4 -15 ms** (Page 354)

▶ 2 - 10 ms

▶ 5-20 ms

▶ 10-25 ms

**Question No: 3 ( Marks: 3 ) - Please choose one**

1-bit sign, 8-bit exponent, 23-bit fraction and a bias of 127 is used for \_\_\_\_\_ Binary Floating Point Representation

▶ Double precision

▶ **Single Precision** (Page 348)

▶ All of above

▶ Half Precision

**Question No: 4 ( Marks: 3 ) - Please choose one**

The average rotational latency if the disk rotated at 20,000rpm is \_\_\_\_\_

▶ 0.5 ms

▶ 3.5 ms

▶ 2.5 ms

▶ **1.5 ms** (Page 324)

**Question No: 5 ( Marks: 3 ) - Please choose one**

A hard disk with 5 platters has 1024 tracks per platter, 512 sectors per track and 512 bytes/sector. What is the total capacity of the disk?

▶ 1.5 GB

▶ **1 GB** (Page 324)

▶ 2 GB

▶ 3 GB

خود کو تمہیں سے بڑھ کر کوئی اچھا مشورہ نہیں دے سکتا